Remarks

Claim 101-116 and 123-223 are pending.

Rejection of Claims under 35 U.S.C. §§ 102(b) and 103(a)

The Examiner rejected Claims 143-145, 147, 149-155, 167-193, and 196-223 under Section 102(b) as anticipated by USP 5,483,094 (Sharma). The Examiner also rejected Claims 146 and 148 under Section 103(a) as obvious over Sharma. These rejections are respectfully traversed.

The Examiner cites Sharma as disclosing all of the elements of the rejected claims, including at least two overlying layers 33, 34 of epitaxial silicon (ES) citing to FIG. 12 and col. 3, line 42. With respect to Claims 146, 148, the Examiner maintains that it would be obvious to use a thickness of the insulative layer of about 5-20 nm or 2-5 nm.

The Examiner's interpretation of Sharma is in error.

Sharma specifically describes a gate structure composed of a *single* epitaxial silicon layer that is *a single crystal*. See, for example, the Abstract, and the Detailed Description at col. 3, lines 1-3 (emphasis added):[1]

> Abstract
>
> An electrically programmable read-only memory cell includes **a single crystal silicon pillar** having the active region of the memory cell...
>
> DETAILED DESCRIPTION OF EMBODIMENTS
>
> The present invention includes a memory cell that has **a single crystal silicon pillar** formed over a buried layer or doped region...

Sharma describes a *single* epitaxial silicon layer comprising two dopant regions within the single layer. This is illustrated by FIG. 3, shown below

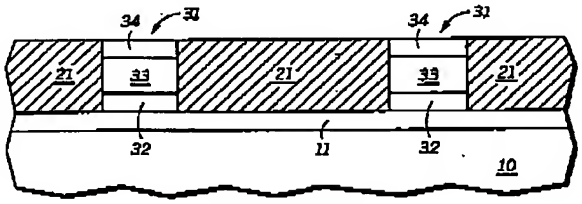

FIG. 3

[1] See also the claims, for example Claim 2: The memory cell of claim 1, wherein the pillar includes *single crystal silicon.*

and described in Sharma at col. 3, line 42 to col. 4, line 27 (emphasis added)

> Silicon pillars 31 are selectively and epitaxially grown from exposed portions of the buried layer 11 lying at the bottoms of the openings 22 as shown in FIG. 3. Each silicon pillar 31 includes *a lower doped region 32* that acts as part of the source region for the memory cell, *a central region 33* that acts as the channel region for the memory cell, and *an upper doped region 34* that acts as the drain region for the memory cell. The regions 32 and 34 are n-type doped, and the central region 33 is p-type doped. *The combination of the regions 32-34 within the silicon pillars 31 acts as the active region for the memory cell.* The doping within the silicon pillars may be performed using in-situ doping that allows more flexibility in the doping levels within the regions 32-34...
>
> In this embodiment, the silicon pillars 31 are formed using a conventional method. The formation may be performed by low pressure chemical vapor deposition using a silicon hydride (silane, disilane, or the like), a silicon-chlorine compound (dichlorosilane or the like), or a combination thereof... The doping levels within regions 32-34 are determined in part by the relative flow rate between the silicon source and the dopant gas. One skilled in the art can adjust the relative gas flow rates to obtain the desired doping concentrations.
>
> Each of the lower and upper doped regions 32 and 34 has a thickness of about 2000 angstroms and a doping concentration no less than about 1E19 ions per cubic centimeter, and each of the central regions 33 has a thickness of about 4000 angstroms and a doping concentration no higher than about 1E17 ions per cubic centimeter.

Thus, the *single crystal* epitaxial silicon layer (i.e., the silicon pillar 31) includes three doped *regions* — *a lower doped region 32, a central region 33, and an upper doped region 3.* Sharma does *not* describe separate and overlying epitaxial layers with each layer comprising a silicon crystal having a surface. Sharma describes a single crystal epitaxial silicon layer 31 comprising three dopant regions.

By comparison, Applicant is claiming a structure having *at least two layers* of epitaxial silicon. *Each* of the at least two epitaxial layers comprises *a single silicon crystal* having a top or upper surface defining a facet, and vertically-oriented and insulated sidewalls. See specification, for example, at page 2 (lines 24-25), page 4 (lines 23-26), page 9 (lines 14-15) and page 11 at lines 21-23, and the Abstract at lines 11-14.[2]

Thus, Applicant's structure comprises at least *two separate and overlying silicon crystals.*

Sharma's description of a single crystal epitaxial layer having different doped regions does not teach or suggest Applicant's structures as claimed. Accordingly, withdrawal of this rejection is respectfully requested.

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[2] Specification at page 4, lines 23-26 (emphasis added): "In one embodiment of a transistor, the transistor gate comprises at least two overlying layers of epitaxially grown silicon, *each epitaxial layer comprising a single*

Information Disclosure Statement.

The Examiner is again requested to return a copy of the Form 1449/PTO, which was submitted in a Supplemental Information Disclosure Statement (with the required fee), in Applicant's response **filed June 6, 2003**. Another copy of this submission is enclosed herewith. Also enclosed is the PTO date-stamped return postcard confirming the timely filing of the IDS on June 6, 2003.

Considerations of the listed references is requested, and return of the previously filed Form 1449/PTO is requested showing the references as being initialed and considered.

Extension of Term. The proceedings herein are for a patent application and the provisions of 37 CFR § 1.136 apply. Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that Applicant has inadvertently overlooked the need for a petition for extension of time. If any extension and/or fee are required, please charge Account No. 23-2053.

Based on the above remarks, the Examiner is respectfully requested to reconsider and withdraw the rejections of the claims. It is submitted that the present claims are in condition for allowance, and notification to that effect is respectfully requested.

Respectfully submitted,

Kristine Strodthoff

Dated: June 29, 2004

Kristine M. Strodthoff
Reg. No. 34,259

WHYTE HIRSCHBOECK DUDEK S.C.
555 East Wells Street
Suite 1900
Milwaukee, Wisconsin 53202-3819
(414) 273-2100

Customer No. 31870

silicon crystal having a top or upper surface defining a facet, preferably having a (100) plane orientation, and vertically oriented and insulated sidewalls..."

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DENOTES RECEIPT ON THE DATE STAMPED OF:

In re Application of	: Ping, et al.
Serial No.	: 10/046,497
Filing Date	: October 26, 2001
For	: Method for Forming Raised Structures by Controlled Selective Epitaxial Growth of Facet Using Spacer
Examiner:	: Le, Thao X.
Group Art Unit	: 2814
Confirmation No.	: 8624
Atty. Docket No.:	: MTI-31041-A

Enclosures: Response After Final (7 pages), Supplement IDS, Form PTO-1449, Check No. 16320 in the amount of $180.00, and Return Postcard

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